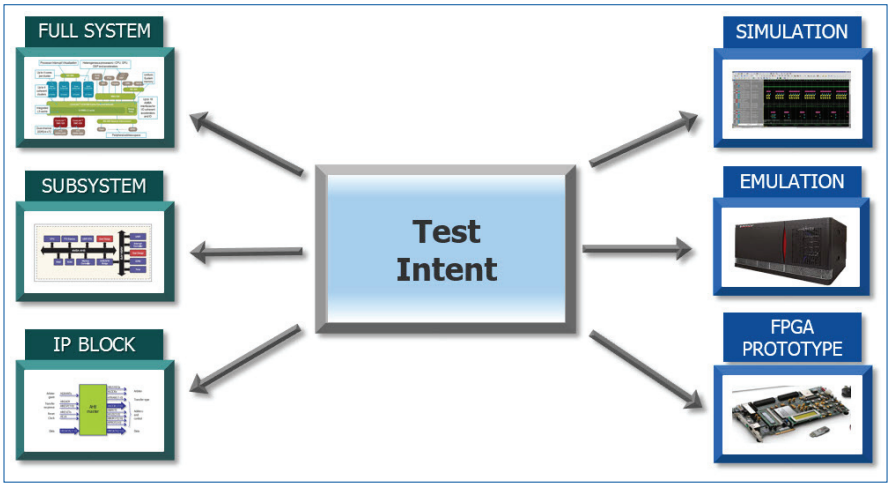
Questa inFact Portable Stimulus



Questa inFact portable stimulus automates test creation from IP to SoC.

Portable Stimulus Overview

Portable stimulus raises the level of verification abstraction and enables users to automate testing of the complex scenarios that emerge in block, subsystem, and SoC level verification. Building on the concept of constraint-based, transaction-level verification (which is already well understood and widely deployed today), portable stimulus provides higher efficiency in test generation and faster coverage closure.

Mentor's Questa® inFact™ was the first successful commercial EDA tool for portable stimulus. Questa inFact reads a single specification of test intent and automatically generates stimulus and coverage for verification at any level, from individual blocks to complete systems. The generated tests span not only every level of the design hierarchy but also many verification platforms, including simulation, emulation, FPGA prototypes, and fabricated chips in the bring-up lab. Tests are tuned for best performance and maximum coverage for each design.

The Questa inFact tool suite offers:

- A graph-based approach to accelerate coverage closure and find more design bugs
- An integrated development environment for editing and visualizing portable stimulus models
- An interactive pre-run debug environment for portable stimulus models
- Tools to import constraints and random variables from SystemVerilog classes

FEATURES AND BENEFITS:

Automatic test generation

- Stimulus, results, and coverage
- Intuitive portable stimulus models

Truly portable tests

- From block to subsystem to SoC level
- Spans simulation, emulation, FPGA prototypes, and fabricated chips
- Tuned for efficiency and efficacy on each verification platform
- Same model used to generate tests on all levels and platforms

Incremental adoption

- Easy to generate complex tests from existing UVM environments
- Direct reuse by importing UVM class fields and constraints
- Model specification builds on familiar concepts from UVM and SystemVerilog

Faster coverage convergence

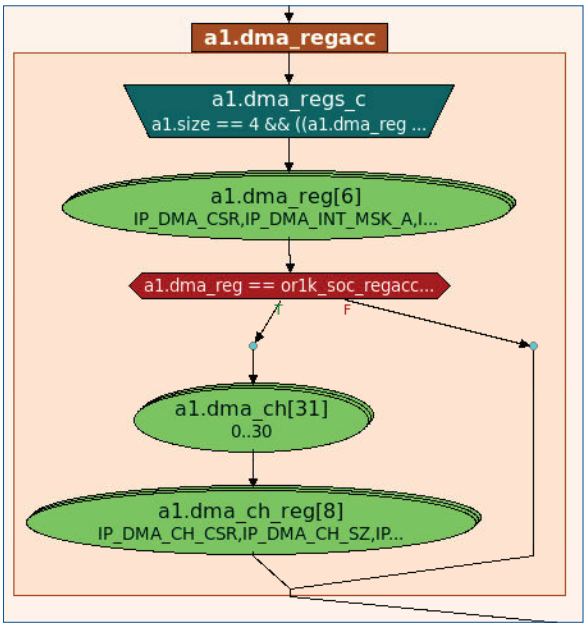
- 10–100x more tests than constrained-random testbenches
- Tests targeted at coverage holes
- No redundant tests

Mature solution

- Questa inFact technology formed the basis for the Accellera Portable Test and Stimulus Standard

Portable Stimulus Models

With the PSS, users capture their test intent in declarative models that encapsulate complex behaviors in a way that can easily be reused and customized. Questa inFact users develop portable stimulus models in an integrated development environment (IDE) that boosts productivity. These models are hierarchical, so a full-chip specification can be composed from models supplied by IP providers. The models support constraints on resource requirements and data exchanges. Questa inFact ensures that the wide range of generated tests obey these constraints and exercise only legal design scenarios.

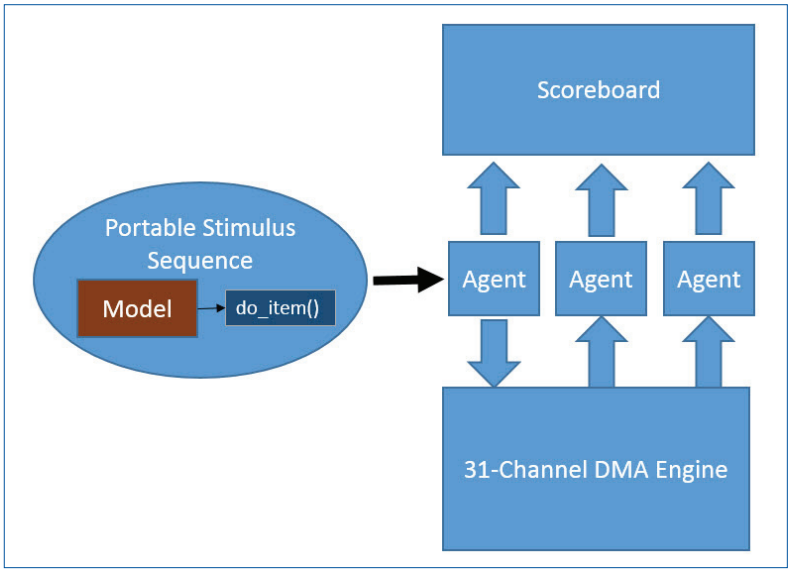


Portable stimulus models can be shown graphically.

Faster Coverage at the Block Level

Applying the portable stimulus at the block level speeds the time to coverage closure, especially when testbenches are compliant with the Universal Verification Methodology (UVM). Questa inFact generates non-redundant tests, resulting in test goals being achieved 10–100x more efficiently than with constrained-random generation. The generated tests run in any simulation environment, including SystemC and VHDL testbenches, even if automated stimulus was not previously available.

Users find bugs more quickly and improve coverage without adding simulation resources. For example, a testbench may exercise a multichannel DMA engine using a UVM sequence as defined by a SystemVerilog descriptor class. Questa inFact converts this class into a portable stimulus model that automatically generates a wider range of test sequences with faster coverage convergence than possible with directed tests and constrained-random stimulus.

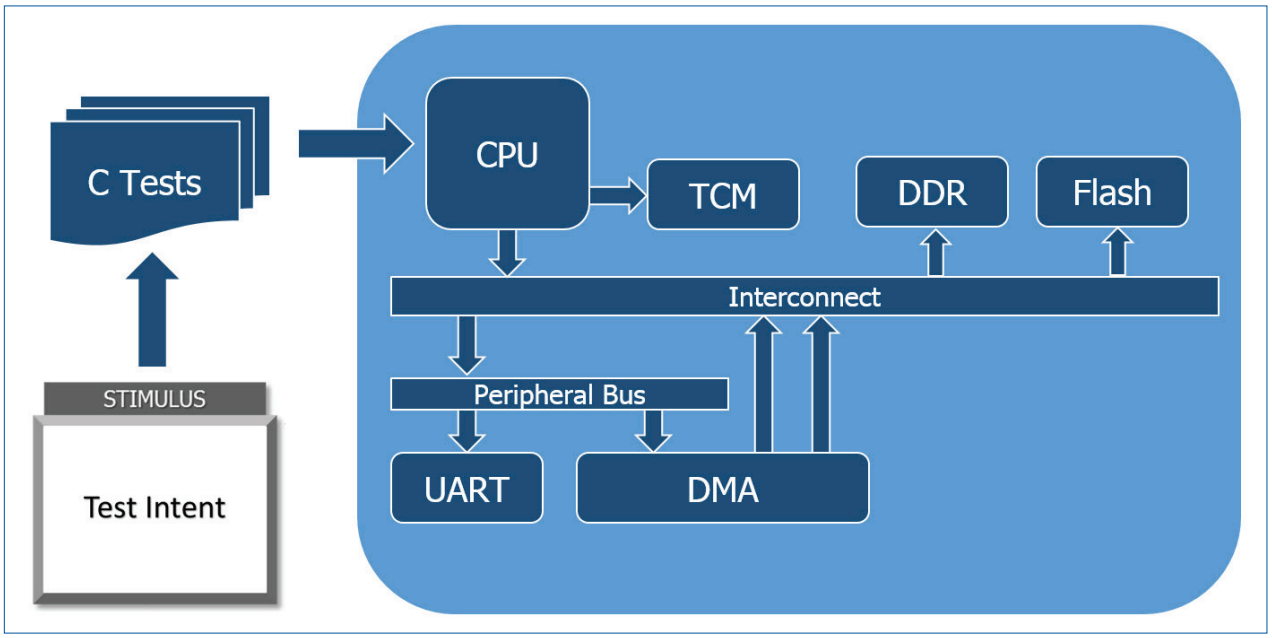


Portable stimulus UVM sequences integrate easily.

Automating Tests for SoC Verification

As verification moves up the design hierarchy, block-level portable stimulus models are combined to orchestrate scenario-level tests across multiple blocks and interfaces. Questa inFact improves verification productivity by generating tests that find corner-case bugs and hit deep coverage points much more efficiently than hand-written or constrained-random tests.

At the SoC level, Questa inFact supports software-driven verification. SoCs, by their very definition, contain one or more embedded processor that controls operation of the design. Questa inFact automatically generates C tests that run on the SoC processors to verify key system-level aspects of the design efficiently and with high coverage. Software-driven verification leverages the same portable stimulus models that are used at the block level.



Portable stimulus automates software-driven SoC level tests.

The generated SoC-level tests are tuned for each platform, including for FPGA prototypes and fabricated chips where no testbench exists. Questa inFact eliminates the need to hand-write C tests and modify them for each platform. The same scenarios can be run from block-level simulation through silicon, leveraging portable stimulus models in multiple ways. Further, scenarios that find bugs at the system level can also generate block-level tests for easier debug. Thus, portability goes both ways: up or down the design hierarchy.

Getting Started with Portable Stimulus

The Verification Academy (www.verificationacademy.org) provides a comprehensive library of resources to help you get started adopting portable stimulus. Organized into a collection of free, online courses, forums, and articles, the Academy brings key aspects of portable stimulus into focus. It starts with basic discussions about the motivations and goals for portable stimulus, exploring the concept of scenario-level stimulus and examining the requirements for a viable portable stimulus. It progresses to advanced courses with examples demonstrating such things as how to easily abstract portable stimulus test intent targeted to a specific design and how to enhance portable stimulus test intent to cover new requirements without modifying the original test-intent description. Each course consists of multiple sessions allowing you to pick and choose topics of interest as well as revisit topics for future reference.

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