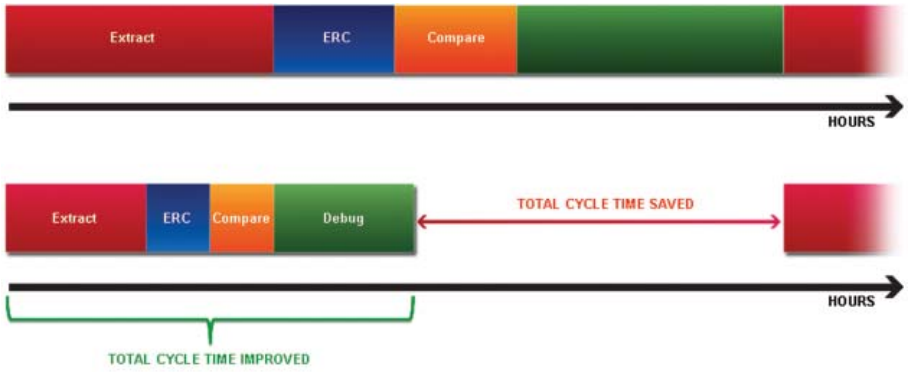
Calibre nmLVS

D A T A S H E E T



Calibre® nmLVS is two to three times faster than traditional layout vs. schematic processes.

Calibre nmLVS — the Next Generation in Circuit Verification

Calibre® nmLVS, the market-leading layout vs. schematic physical verification tool, is tightly linked with both Calibre nmDRC and Calibre xRC to deliver production-proven device extraction for both physical verification and parasitic extraction. Calibre nmLVS performs a vital function as a member of a complete IC verification tool suite by providing device and connectivity comparisons between the IC layout and the schematic. Calibre's hierarchical processing engine runs Calibre nmLVS, supplying data for modifying the IC design to achieve superior functionality and reliability. Calibre nmLVS enables accurate circuit verification because it is able to measure actual device geometries on a full-chip for a complete accounting of physical parameters. These precise device parameters supply the information for back-annotation to the source schematic and the comprehensive data for running simulations. In addition to working with Calibre xRC, Calibre nmLVS can also be used with third party parasitic extraction tools.

Calibre's ability to interactively verify and make corrections in an existing design framework, without being constrained by proprietary tools or flows, dramatically reduces iteration runtime and error debugging. This robust and easy-to-use integration enables designers to use Calibre as a single platform for cell/block and full-chip verification, as well as parasitic extraction.

Faster Cycle Time

Improved extraction for advanced stress parameters (especially at 45 nm and below), electrical rule checking capability, comparison that now takes only minutes, and an improved, easy to use debugging environment reduces the overall time spent in LVS. The ability to use hierarchical design and hardware scaling further reduces your verification time.

Benefits of Ownership

- ***Market Leadership*** — Calibre nmLVS continues to lead the market. Preferred by engineers and management for its proven performance, capacity, reliability and debug ease-of-use.
- ***Best-in-Class Accuracy*** — Device recognition accuracy is crucial for tape-out success. Calibre nmLVS delivers the trusted device recognition accuracy and timely execution required for world-class silicon delivery.
- ***Fast Runtime*** — Automated proprietary hierarchical and logic injection technologies provide virtually unlimited design scope with fast runtimes. Multi-threaded and distributed CPU processing capabilities ensure future proof scaling on your hardware.
- ***Flexibility*** — Calibre nmLVS is ideally suited for processing any size job requiring intricate device parameter extraction, whether it's an analog/RF design or a multi-million gate IC.
- ***Reliability*** — With thousands of users, Calibre nmLVS sets the standard for reliability and predictability in all operations.
- ***Design Debugging and Ease-of-Use*** — Calibre nmLVS provides an intuitive and easy-to-use integrated design verification debugging environment to help you find and fix design issues.

Mentor Graphics®

Complete LVS Verification Solution from 130 to 45 nm

Calibre nmLVS provides best-in-class device recognition and parameter extraction for source netlist comparison, and its robust and easy-to-use integration lets you insert Calibre nmLVS into your design flow, allowing you to use Calibre as a single platform for cell/block and full-chip verification.

Customers who are designing at the cutting edge of 45 nm can use Calibre to extract all the new advanced stress parameters that are required to do accurate modeling at that process node. At 45 nm, extracting advanced stress parameters, applying design-for-manufacturing checks, and performing electrical as well as topological design rule checks during the layout vs. schematic (LVS) process is a must. Calibre nmLVS makes this possible, saving you time and money.

Superior Device Extraction and Analysis

Both analog and digital device extraction require comprehensive and accurate device extraction capabilities. Calibre nmLVS provides automatic device recognition and parameter extraction for standard devices with typical BSIM3/4 and PSP parameters, as well as a user-defined option when more complex requirements are needed. In both cases, Calibre nmLVS can extract parameters using standard SVRF or TCL-based rules. See table for the required measurements that nmLVS provides.

Advanced Device Parameters

As transistor sizes continue to decrease, the complexity and number of parameters that are required for extraction are increasing. At 45 nm and below, foundries are extracting custom parameters that are important to their unique process. With the ability to create user-defined parameters for extraction, nmLVS is “future-proof” and ready for the unknown at 32 nm and below. Calibre nmLVS goes beyond where older generation LVS tools break down at 45 nm because they cannot extract parameters involving more than one transistor.

Comprehensive Debugging

Time spent in debugging can dramatically affect time to tape-out, but incomplete debugging can result in yield failures. Calibre nmLVS provides a thorough scope of debugging and analysis functionality integrated into a user-friendly environment that helps you find and fix layout vs. schematic issues quickly and effectively. Full cross-probing of SPICE netlists, with browser and netlist comparison, is available, as is identification of shorts and isolation.

Process Node	Required Measurements
180–150 nm	W, L, AS, AD, PD, PS (BSIM3)
130 nm	SA, SB (BSIM4/PSP)
90–65 nm	SCA, SCB (BSIM4/PSP)
45 nm	Active spacing, poly spacing, custom measurements
32 nm	Finfet support nmLVS is ready for new, custom measurements

The graphical environment is easy to use and includes design-fix suggestions and visual indication of the location of geometrical and electrical violations, such as shorts in the layout. A dynamic results-viewing environment allows you to see violations and start fixing them as soon as they are detected, rather than waiting until the DRC run completes.

Programmable Electrical Rule Checking

Calibre nmLVS can now be enhanced with Calibre PERC (Programmable Electrical Rule Checker). With Calibre PERC, you can automate advanced, customer-specific ERCs to eliminate lengthy and error-prone manual checking. PERC recognizes grouped devices that are connected as you describe and measures geometrical data associated with the circuit topology.

Calibre PERC can be used in combination with Calibre nmLVS to find design errors not identified by traditional tools. You can run multiple electrical rule checks independently or together, using either standard rules from the foundry, or your own unique custom rules. You can easily insert electrical rule checks into your design flow using Calibre PERC as part of an integrated Calibre platform for cell, block, and full-chip verification. This capability is not available from any other tool today.

Fully Scalable Solution

Calibre nmLVS allows you to maximize your resources and minimize the time to complete verification by taking advantage of design hierarchy and using hardware scaling on local and remote machines.

Hierarchical Design Methodology

Calibre nmLVS reduces your turn-around time for IC verification with a logic injection technology that automatically scans for repeated and common device patterns. By recognizing repeated hierarchy in your design, Calibre nmLVS

can simplify the repeated devices and “inject” a level of hierarchy it then uses during the comparison process.

Hardware Scaling

Calibre nmLVS also enables MT, MTFlex, and Hyperscaling to maximize hardware and software resource use. Multiple technologies that can scale for efficient and effective use of your hardware and allow for growth is one of the many benefits of the Calibre platform.

Calibre: The Gold Standard

Foundries and integrated device manufacturers (IDMs) have proven the excellence of Calibre nmLVS through their unprecedented support of Calibre’s device extraction, comparison, and debugging technology. Direct support of the Calibre rules by the foundries and IDMs provides comprehensive coverage for your process nodes, and you have access to the rules that ensure first-pass silicon success. Our strong relationship with your manufacturer makes the decision to use Calibre technology a low-risk choice.

Platforms Supported

32 and 64 bit Linux Redhat, SUN Solaris

Visit our website at www.mentor.com

Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon
97070-7777
Phone: 503-685-7000
Fax: 503-685-1204

Sales and Product Information
Phone: 800-547-3000

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

North American Support Center
Phone: 800-547-4303

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics Taiwan
Room 1001, 10F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-87252000
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140 -0001
Japan
Phone: 81-3-5488-3033
Fax: 81-3-5488-3004

08-08-MGC 4421:080213